NTS4101P

Power MOSFET

−20 V, −1.37 A, Single P−Channel, SC−70

Features

- Leading −20 V Trench for Low $R_{DS(on)}$
- −2.5 V Rated for Low Voltage Gate Drive
- SC−70 Surface Mount for Small Footprint (2x2 mm)
- Pb−Free Package is Available

Applications

- High Side Load Switch
- Charging Circuit
- Single Cell Battery Applications such as: Cell Phones, Digital Cameras, PDAs

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Units
Drain−to−Source Voltage			V_{DSS}	−20	V
Gate−to−Source Voltage			V_{GS}	±8	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−1.37	A
		T_A = 70°C		−0.62	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	0.329	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	−4.0	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode), Continuous			I_S	−0.5	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	380	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

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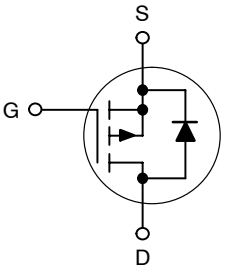
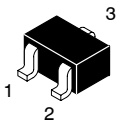
$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max
−20 V	83 mΩ @ −4.5 V	−1.37 A
	88 mΩ @ −3.6 V	
	104 mΩ @ −2.5 V	

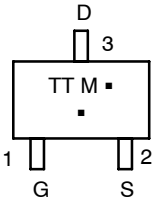
P−Channel MOSFET



MARKING DIAGRAM & PIN ASSIGNMENT



SC−70/SOT−323
CASE 419
STYLE 8



TT = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NTS4101PT1	SOT−323	3000/Tape & Reel
NTS4101PT1G	SOT−323 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−20	−24.5		V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				−13.7		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −16 V	T_J = 25°C			−1.0	μA
			T_J = 70°C			−5.0	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−0.45	−0.64	−1.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				2.7		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V, I_D = −1.0 A			83	120	mΩ
		V_{GS} = −3.6 V, I_D = −0.7 A			88	130	
		V_{GS} = −2.5 V, I_D = −0.3 A			104	160	
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −20 V			603	840	pF
Output Capacitance	C_{OSS}				90	125	
Reverse Transfer Capacitance	C_{RSS}				62	85	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −4.5 V, I_D = −1.0 A			6.4	9.0	nC
Threshold Gate Charge	$Q_{G(TH)}$				0.7		
Gate−to−Source Charge	Q_{GS}				1.0		
Gate−to−Drain Charge	Q_{GD}				1.5		
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −4.5 V, V_{DD} = −4.0 V, I_D = −1.0 A, R_G = 6.2 Ω			6.2	12	ns
Rise Time	t_r				14.9	25	
Turn−Off Delay Time	$t_{d(OFF)}$				26	40	
Fall Time	t_f				18	30	
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −0.3 A	T_J = 25°C		−0.61	−1.2	V
			T_J = 125°C		−0.5		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_{SD}/dt = 100 A/μs, I_S = −1.0 A			10.9	20	ns
Charge Time	T_a				7.1		
Discharge Time	T_b				3.8		
Reverse Recovery Charge	Q_{RR}				4.25		nC

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

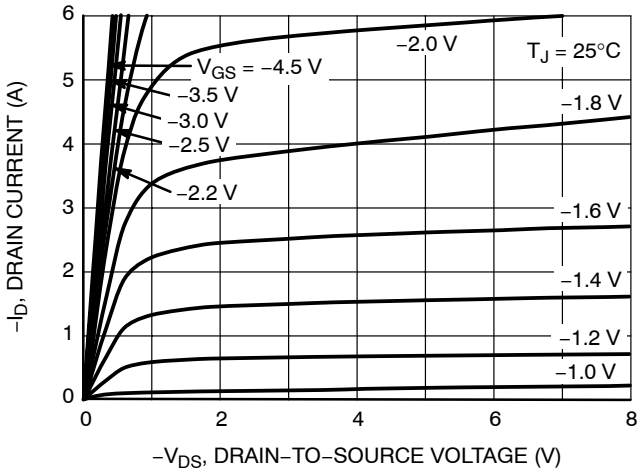


Figure 1. On−Region Characteristics

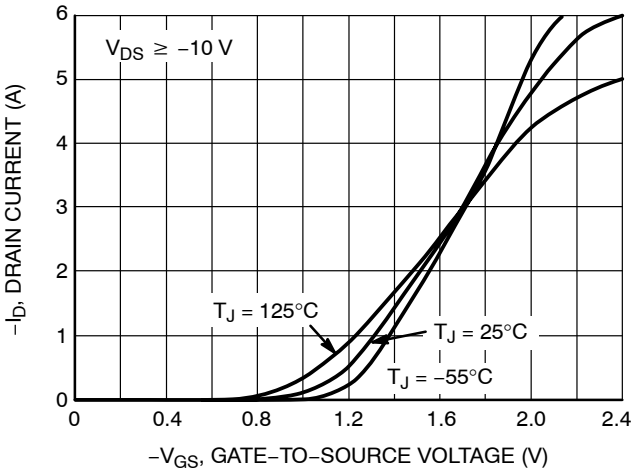


Figure 2. Transfer Characteristics

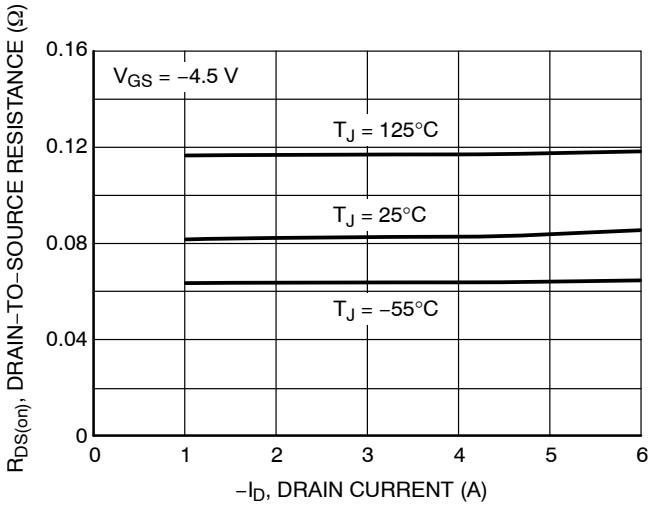


Figure 3. On−Resistance versus Drain Current and Temperature

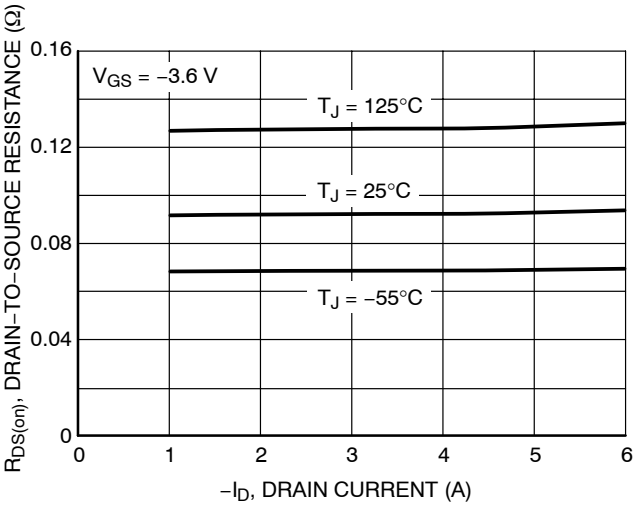


Figure 4. On−Resistance versus Drain Current and Temperature

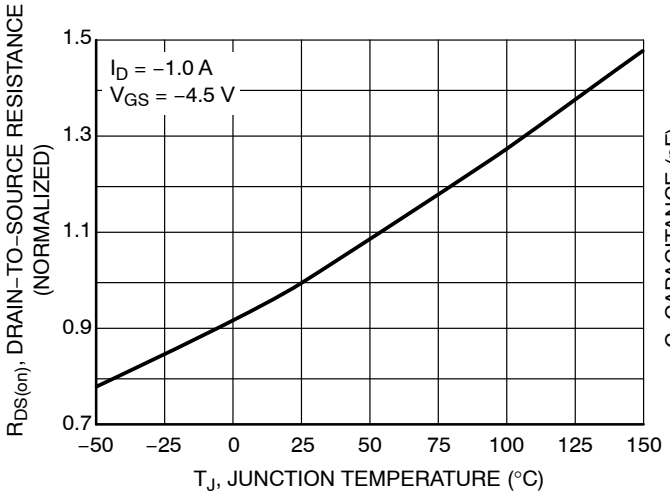


Figure 5. On−Resistance Variation with Temperature

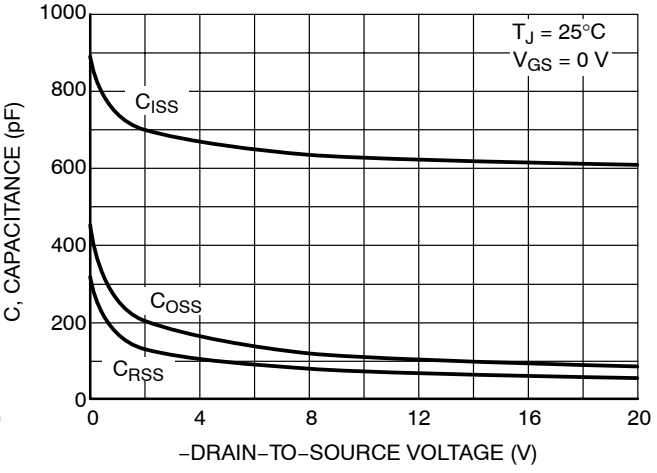


Figure 6. Capacitance Variation

TYPICAL CHARACTERISTICS

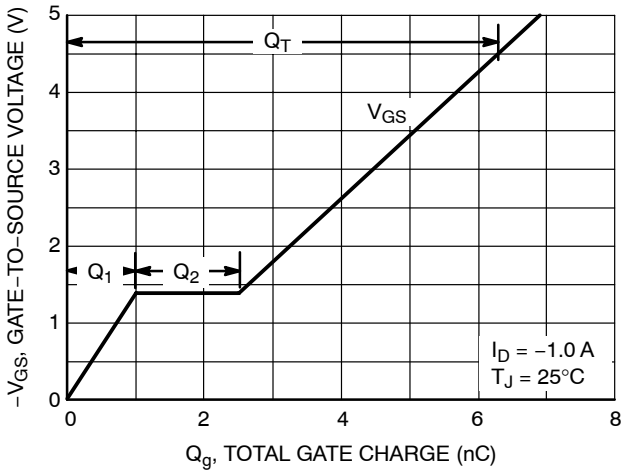


Figure 7. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

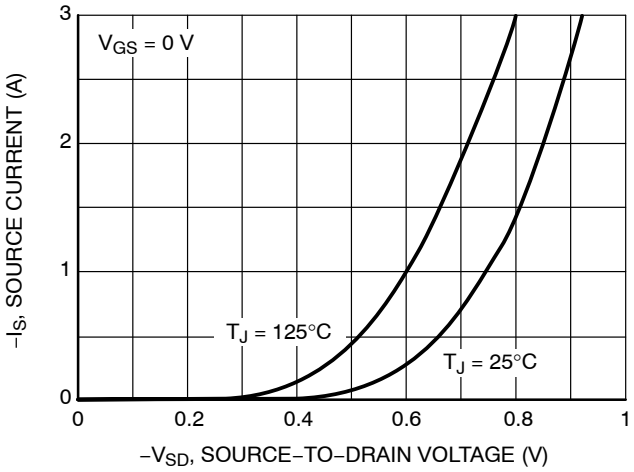
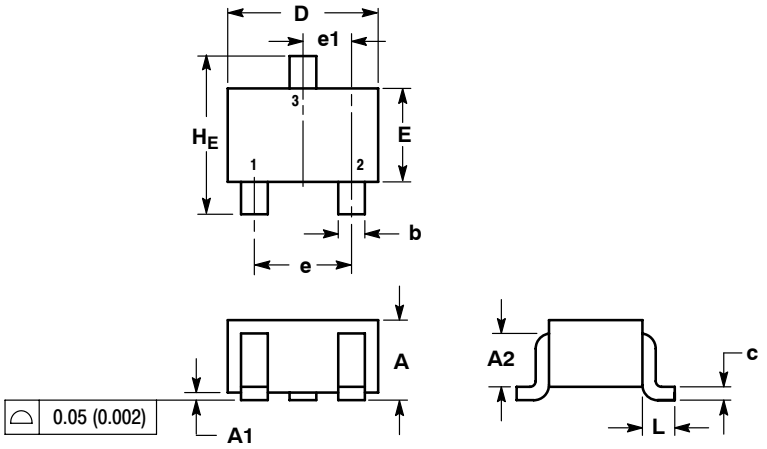


Figure 8. Diode Forward Voltage versus Current

PACKAGE DIMENSIONS

SC−70 (SOT−323)
CASE 419−04
ISSUE M

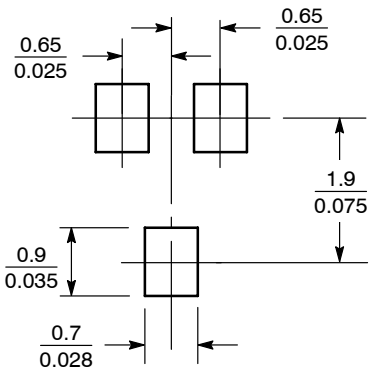


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2		0.7 REF			0.028 REF	
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1		0.65 BSC			0.026 BSC	
L		0.425 REF			0.017 REF	
H_E	2.00	2.10	2.40	0.079	0.083	0.095

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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